US005990021A

United States Patent [19]

Prall et al.

[11] Patent Number: 5,990,021

[45] Date of Patent: Nov. 23, 1999

[54] **INTEGRATED CIRCUIT HAVING SELF-ALIGNED CVD-TUNGSTEN/TITANIUM CONTACT PLUGS STRAPPED WITH METAL INTERCONNECT AND METHOD OF MANUFACTURE**

[75] Inventors: **Kirk Prall**; **Howard E. Rhodes**; **Sujit Sharan**; **Gurtel Sandhu**, all of Boise; **Philip J. Ireland**, Nampa, all of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **08/994,950**

[22] Filed: **Dec. 19, 1997**

[51] **Int. Cl.**[6] **H01L 21/336**

[52] **U.S. Cl.** **438/745**; 438/745; 438/754; 438/755; 438/756; 438/757; 438/753

[58] **Field of Search** 438/745, 754, 438/755, 756, 757, 753

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,032,530 7/1991 Lowrey et al. 437/34

5,134,085 7/1992 Gilgen et al. 437/52

5,846,881 12/1998 Sandhu et al. 438/683

Primary Examiner—Benjamin Utech

Assistant Examiner—Lan Vinh

Attorney, Agent, or Firm—Trask, Britt & Rossa

[57] **ABSTRACT**

This invention is a process for manufacturing a random access memory array. Each memory cell within the array which results from the process incorporates a stacked capacitor, a silicon nitride coated access transistor gate electrode, and a self-aligned high-aspect-ratio digit line contact having a tungsten plug which extends from the substrate to a metal interconnect structure located at a level above the stacked capacitor. The contact opening is lined with titanium metal which is in contact with the substrate, and with titanium nitride that is in contact with the plug. Both the titanium metal and the titanium nitride are deposited via chemical vapor deposition reactions.

11 Claims, 7 Drawing Sheets